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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/781,707	COLE ET AL.
	Examiner	Art Unit
	Ida M. Soward	2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-68* is/are pending in the application.

4a) Of the above claim(s) *47-68* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,11-18,23-30,32,37-41 and 43-46* is/are rejected.

7)☒ Claim(s) *7-10,19-22,31,33-36 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed February 20, 2004.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-46, drawn to an integrated circuit, classified in class 257, subclass 328.

II. Claims 47-68, drawn to a method of forming a structure, classified in class 438, subclass 212.

The inventions are distinct, each from the other because of the following reasons: Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). Unpatentability of the Group I invention would not necessarily imply unpatentability of the Group II invention, since the device of the Group I invention could be made by a process materially different from those/that of the Group II invention. In the instant case, the method of forming a structure as claimed can be used to make other and materially different product, such as a photodiode or a photogate structure.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Gabriela Coman on August 4, 2005 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-46. Affirmation of this election must be made by applicant in replying to this Office action. Claims 47-68 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 24-37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 24, it is not understood what is below the substrate... the extension of the trench or the base layer.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 12-14, 23-26 and 29-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Clevenger et al. (US 2004/0227061 A1).

In regard to claim 1, Clevenger et al. teach an integrated circuit comprising: a substrate 100 comprising a lower layer 100A and an upper layer 100B on the lower layer 100A; an array of pixel cells at a surface of the upper layer 100B, each pixel cell 104A & 104B comprising a photo-conversion device; and a trench structure around at least a portion of the array, wherein the trench structure 116A & 116B extends from the surface to the lower layer 100A, and wherein the trench structure 116A & 116B prevents at least a portion of photons or charged particles from passing through the trench structure to the array (Figure 12, pages 3-4, paragraphs [0039]-[0052]).

In regard to claims 12 and 23, Clevenger et al. teach the integrated circuit comprises of a CMOS image sensor (pages 1, paragraphs [0004]).

In regard to claim 13, Clevenger et al. teach a structure for isolating an active area of an integrated circuit, the structure comprising: a trench 116A & 116B formed in a

substrate 100 of the integrated circuit along at least a portion of a periphery of the active area, the substrate 100 having a lower layer 100A and an upper layer 100B on the lower layer 100A, wherein the trench 116A & 116B extends from a surface of the upper layer 100B to a surface of the lower layer 100A; an insulating liner 118B formed along sidewalls of the trench 116A & 116B; and a first fill material 120 formed over the insulating liner 118B wherein the first fill material 120 at least partially fills the trench 116A & 116B and prevents at least a portion of photons and electrons from passing through the trench to the active area (abstract) (Figure 12, pages 3-4, paragraphs [0039]-[0052]).

In regard to claims 14 and 26, Clevenger et al. teach the insulating liner 118B being a high absorption material (page 2, paragraph [0036]).

As best understood and in regard to claim 24, Clevenger et al. teach a structure for isolating an active area on an integrated circuit, the structure comprising: a plurality of trenches 116A & 116B formed in a substrate 100B of the integrated circuit on at least a portion of a periphery of the active area, wherein each of the plurality of trenches 116A & 116B extends to a surface of a base layer 100A below the substrate 100B (Figure 12, pages 3-4, paragraphs [0039]-[0052]).

In regard to claim 25, Clevenger et al. teach an insulating liner 118B formed along each sidewall of the plurality of trenches 116A & 116B (Figure 12, pages 3-4, paragraphs [0039]-[0052]).

In regard to claim 29, Clevenger et al. teach a first fill material 120 that at least partially fills each of the plurality of trenches 116A & 116B and prevents at least a

portion of photons or charges particles from passing through the trench (abstract) (Figure 12, pages 3-4, paragraphs [0039]-[0052]).

In regard to claim 30, Clevenger et al. teach the insulating liner 118B being a high absorption material (page 2, paragraph [0036]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-4, 11, 18, 37 and 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clevenger et al. (US 2004/0227061 A1) in view of Rhodes (US 2003/0089929 A1).

In regard to claim 44, Clevenger et al. teach an isolation structure 116A & 116B provided at a surface of a substrate 100A between a source area in which at least one of photons and charged particles originate and an active region, the isolation structure 116A & 116B comprising: a length extending across the surface of the substrate between the source area and the active area (Figure 12, pages 3-4, paragraphs [0039]-[0052]).

In regard to claim 45, Clevenger et al. teach an integrated circuit comprising: a substrate 100; an array of pixel cells at a surface of the substrate 100, each pixel cell

comprising a photo-conversion device (title and abstract); and at least one trench 116A & 116B around at least a portion of the array (Figure 12, pages 3-4, paragraphs [0039]-[0052]).

However, Clevenger et al. fail to teach at least one trench extending from the surface of the substrate into the substrate to a depth of at least about 0.5μm.

Rhodes teaches at least one trench extending from the surface of the substrate into the substrate to a depth of at least about 0.05 to 10 μm (page 6, paragraph [0056]) which overlap 0.5μm and 4μm to 6μm.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the IC isolation structure as taught by Clevenger et al. with the IC isolation structure having at least one trench extending from the surface of the substrate into the substrate to a depth of at least about 0.05 to 10 μm as taught by Rhodes to provide an improved semiconductor imaging device (page 1, paragraph [0001]).

In regard to claim 2, Rhodes et al. further teach the trench structure having sidewalls and containing a first material 26 that prevents at least a portion of photons or charged particles from passing through the trench structure to the array (Figure 5, page 4, paragraph [0040]).

In regard to claim 3, Rhodes et al. teach a liner 100 formed along at least a portion of the sidewalls (Figure 5, page 4, paragraph [0040]).

In regard to claim 4, Clevenger et al. teach the insulating liner 118B being a high absorption material (page 2, paragraph [0036]).

Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clevenger et al. (US 2004/0227061 A1) and Rhodes (US 2003/0089929 A1) as applied to claims 1 and 12-13 above, and further in view of Yoshinori (JP PAT-NO 363009968 A).

Clevenger et al. and Rhodes teach all mentioned in the rejection above.

However, Clevenger et al. and Rhodes fail the teach a thermal oxide on the sidewalls of the trench structure; and the first material selected from the group consisting of loped polysilicon, undoped polysilicon and boron-doped carbon.

Yoshinori teaches a thermal oxide 26 material of the sidewalls of the trench; and a first fill material 27 comprising an undoped polysilicon, which is an attenuating material that absorbs photons (abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the IC isolation structure as taught by Clevenger et al. and the IC isolation structure having at least one trench extending from the surface of the substrate into the substrate to a depth of at least about 0.05 to 10 μm as taught by Rhodes with the IC isolation structure having a thermal oxide material of the sidewalls of the trench, and a first fill material comprising an undoped polysilicon, which is an attenuating material that absorbs photons as taught by Yoshinori to provide an image sensor capable of electrostatic induction (title).

Claims 15-17, 27 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clevenger et al. (US 2004/0227061 A1) as applied to claims 1, 12-14, 23-26 and 29-30 above, and further in view of Yoshinori (JP PAT-NO 363009968 A).

Clevenger et al. teach all mentioned in the rejection above.

However, Clevenger et al. fail to teach a thermal oxide material of the sidewalls of the trench; and a first fill material comprising an undoped polysilicon, which is an attenuating material that absorbs photons.

Yoshinori teaches a thermal oxide 26 material of the sidewalls of the trench; and a first fill material 27 comprising an undoped polysilicon, which is an attenuating material that absorbs photons (abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the IC isolation structure as taught by Clevenger et al. with the IC isolation structure having a thermal oxide material of the sidewalls of the trench, and a first fill material comprising an undoped polysilicon, which is an attenuating material that absorbs photons as taught by Yoshinori to provide an image sensor capable of electrostatic induction (title).

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Clevenger et al. (US 2004/0227061 A1) as applied to claims 1, 12-14, 23-26 and 29-30 above, and further in view of Yu et al. (US 6,225,171 B1).

Clevenger et al. teach all mentioned in the rejection above.

However, Clevenger et al. fail to teach the insulating liner comprising a nitride material or alpha carbon material.

Yu et al. teach the insulating liner 25 comprising a nitride material (Figure 1e, column 4, lines 50-51).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the IC isolation structure as taught by Clevenger et al. with the IC isolation structure having an insulating liner comprising a nitride material as taught by Yu et al. to reduce stresses due to lattice mismatch (column 4, lines 50-57).

Claims 38-39 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clevenger et al. (US 2004/0227061 A1) in view of Fossum (US 2004/0195592 A1).

In regard to claim 38 Clevenger et al. teach an integrated circuit comprising a structure for isolating an active area on the integrated circuit, the structure comprising: a trench 116A & 116B formed in a substrate 100B on at least a portion of a periphery of the active area of the integrated circuit, wherein the trench 116A & 116B extends to a surface of a base layer 100A below the substrate 100B, and wherein the trench 116A & 116B has sidewalls; an insulating liner 118B formed along the sidewalls; and a first fill material 120 formed over the insulating liner 118B that at least partially fills the trench 116A & 116B and prevents at least a portion of photons or electrons from passing through the trench 116A & 116B (Figure 12, pages 3-4, paragraphs [0039]-[0052]).

However, Clevenger et al. fail to teach a processing system, the processing system comprising: a processor; and an integrated circuit coupled to the processor.

Fossum teaches a processing system 600, the processing system 600 comprising: a processor 664; and an integrated circuit 642 coupled to the processor 664 (Figure 10, page 4, paragraphs [0046]-[0047]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the IC isolation structure as taught by Clevenger et al. with the semiconductor structure having a processing system, the processing system comprising: a processor; and an integrated circuit coupled to the processor as taught by Fossum to integrate a processor and an integrated circuit on a single chip (page 4, paragraph [0047]).

In regard to claim 39, Clevenger et al. teach the insulating liner 118B being a high absorption material (page 2, paragraph [0036]).

In regard to claim 43, Clevenger et al. teach the integrated circuit comprises of a CMOS image sensor (pages 1, paragraphs [0004]).

Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Clevenger et al. (US 2004/0227061 A1) and Fossum (US 2004/0195592 A1) as applied to claims 15-16 and 27 above, and further in view of Yoshinori (JP PAT-NO 363009968 A).

Clevenger et al. and Fossum teach all mentioned in the rejection above.

However, Clevenger et al. and Fossum fail to teach the first fill material selected form the group consisting of doped polysilicon, undoped polysilicon and boron-doped carbon.

Yoshinori teaches a thermal oxide 26 material of the sidewalls of the trench; and a first fill material 27 comprising an undoped polysilicon, which is an attenuating material that absorbs photons (abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the IC isolation structure as taught by Clevenger et al. and the semiconductor structure having a processing system, the processing system comprising: a processor; and an integrated circuit coupled to the processor as taught by Fossum with the IC isolation structure having a thermal oxide material of the sidewalls of the trench, and a first fill material comprising an undoped polysilicon, which is an attenuating material that absorbs photons as taught by Yoshinori to provide an image sensor capable of electrostatic induction (title).

Claims 41 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clevenger et al. (US 2004/0227061 A1) and Fossum (US 2004/0195592 A1) in view of Rhodes (US 2003/0089929 A1).

Clevenger et al. teach an integrated circuit comprising a structure for isolating an active area on the integrated circuit, the structure comprising: a trench 116A & 116B formed in a substrate 100B on at least a portion of a periphery of the active area of the integrated circuit, wherein the trench 116A & 116B extends to a surface of a base layer

100A below the substrate 100B, and wherein the trench 116A & 116B has sidewalls; an insulating liner 118B formed along the sidewalls; and a first fill material 120 formed over the insulating liner 118B that at least partially fills the trench 116A & 116B and prevents at least a portion of photons or electrons from passing through the trench 116A & 116B (Figure 12, pages 3-4, paragraphs [0039]-[0052]).

Fossum teaches a processing system 600, the processing system 600 comprising: a processor 664; and an integrated circuit 642 coupled to the processor 664 (Figure 10, page 4, paragraphs [0046]-[0047]).

However, Clevenger et al. and Fossum fail to teach a trench extending from a surface of a substrate to a depth of at least about 0.5μm into the substrate.

Rhodes teaches a trench extending from a surface of a substrate 100B to a depth of at least about 0.05 to 10 μm (page 6, paragraph [0056]) into the substrate 100B, which overlap 0.5μm and 4μm to 6μm.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the IC isolation structure as taught by Clevenger et al. and the semiconductor structure having a processing system, the processing system comprising: a processor; and an integrated circuit coupled to the processor as taught by Fossum with the IC isolation structure having at least one trench extending from the surface of the substrate into the substrate to a depth of at least about 0.05 to 10 μm as taught by Rhodes to provide an improved semiconductor imaging device (page 1, paragraph [0001]).

Allowable Subject Matter

Claims 7-10, 19-22, 31, 33-36 and 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to CMOS image sensors:

Holm et al. (5,501,990) Hong (US 2005/0121708 A1)

Patrick (US 2004/0188727 A1) Sarace (4,416,050)

Yaung et al. (US 2004/0075110 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
August 21, 2005

John M. Howard
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